REMARKS

Claims 1-8, 10, 13-14, 16-19, 21-23, 25, and 28-29 are pending. The Office Action dated January 3, 2007, in this Application has been carefully considered. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1-4, 6-8, 10, 16-19, 21-23, 25, and 28-29 have been amended, and claims 9, 11, 12, 15, 20, 24, 26, 27, and 30 have been cancelled in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

Claims 1-30 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. More specifically, regarding the independent claims 1 and 16, the Examiner stated that although the claims recite "multiplexers," the claims failed to recite the desired output(s) of the multiplexers. In response thereto, Applicant notes that independent claims 1 and 16 are amended herein. Amended claim 1 recites:

1. An apparatus for computing a result of a floating-point operation, wherein the apparatus receives an aligned addend comprising a plurality of bits and a plurality of products, the apparatus comprising:

a compound incrementer coupled to receive at least some of the plurality of bits of the aligned addend and a control signal, and configured to produce an output dependent upon the received bits of the aligned addend and the control signal;

a compression counter coupled to receive at least some of the plurality of bits of the aligned addend and the products and configured to produce an output dependent upon the received bits of the aligned addend and the received products;

a compound adder coupled to receive the output of the compression counter and configured to produce an output dependent upon the output of the compression counter;

a carry network coupled to receive sign bits of the products and the output of the compression counter and configured to produce an output signal and a carry signal dependent upon the received sign bits of the products and the received output of the compression counter;

a selector coupled to receive at least some of the plurality of bits of the aligned addend and the output signal and the carry signal produced by the carry network, wherein the selector is configured to produce a selection signal dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal; and

a plurality of multiplexers (muxes) coupled to receive the output of the compound incrementer, the output of the compound adder, and the selection signal produced by the selector, and configured to produce the result by selecting between the received output of the compound incrementer and the received output of the compound adder dependent upon the selection signal produced by the selector.

Amended claim 16 recites:

16. A computer program product for computing a result of a floating-point operation, wherein the computer program product receives an aligned addend comprising a plurality of bits and a plurality of products, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer readable program code means for operating as a compound incrementer, wherein the compound incrementer receives at least some of the plurality of bits of the aligned addend and a control signal, and produces an output dependent upon the received bits of the aligned addend and the control signal;

computer readable program code means for operating as a compression counter, wherein the compression counter receives at least some of the plurality of bits of the aligned addend and

the products and produces an output dependent upon the received bits of the aligned addend and the received products;

computer readable program code means for operating as a compound adder that receives the output of the compression counter and produces an output dependent upon the output of the compression counter;

computer readable program code means for operating as a carry network, wherein the carry network receives sign bits of the products and the output of the compression counter and produces an output signal and a carry signal dependent upon the received sign bits of the products and the received output of the compression counter;

computer readable program code means for operating as a selector, wherein the selector receives at least some of the plurality of bits of the aligned addend and the output signal and the carry signal produced by the carry network, and wherein the selector produces a selection signal dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal; and

computer readable program code means for operating as a plurality of multiplexers (muxes), wherein the plurality of muxes receive the output of the compound incrementer, the output of the compound adder, and the selection signal produced by the selector, and produce the result by selecting between the received output of the compound incrementer and the received output of the compound adder dependent upon the selection signal produced by the selector.

Applicant believes the output(s) of the multiplexers are adequately described in the amended independent claims 1 and 16.

Claims 1-30 were rejected under 35 U.S.C. 101 as being drawn to non-statutory subject matter. In the Office action, the Examiner stated that "Since there is no physical transform to

establish a practical application, a useful, concrete and tangible result appears to be lacking. Therefore, claims 1-30 are drawn to a non-statutory process."

Applicant respectfully traverses this rejection. Applicant notes that the instant application is entitled "HIGH SPEED ADDER DESIGN FOR A MULTIPLY-ADD BASED FLOATING POINT UNIT," and the Background section of the instant application clearly states:

"The present invention relates generally to a high-speed floating-point adder (adder) and, more particularly, to the improvement of some of the most time critical elements that exist in the adder, such as the end-around-carry-logic."

"Floating-Point Units (FPU) are well known, and have been an element of computer architecture for a number of years."

"...there is a need for a method and/or apparatus to streamline each of the processes that make both evaluations and calculations that address at least some of the problems associated with conventional methods and apparatuses for floating point computations."

The instant applications includes two independent claims -- claims 1 and 16 -- and all other pending claims depend from claims 1 and 16. Independent claim 1 (amended herein) is directed to "An apparatus for computing a result of a floating-point operation..." and comprises tangible elements that work together to produce the result. Applicant asserts that the apparatus of claim 1 is tangible and has utility in at least the computing arts.

Independent claim 16 (amended herein) is directed to "A computer program product for computing a result of a floating-point operation..." having "...a medium with a computer program embodied thereon." Applicant asserts that the computer program product of claim 16 is tangible and has utility in at least the computing arts.

Regarding the rejection of all claims under 35 U.S.C. 101 as being drawn to non-statutory subject matter, Applicant requests that the Examiner either withdraw the rejection or elaborate on the basis of the rejection for each rejected claim.

In the present response, Applicant addresses all of the claim objections and rejections cited in the Office Action. In view of the amendments to the claims and Applicant's remarks, Applicant believes pending claims 1-8, 10, 13-14, 16-19, 21-23, 25, and 28-29 are in condition for allowance, and respectfully request allowance of pending claims 1-8, 10, 13-14, 16-19, 21-23, 25, and 28-29.

With the amendments to the claims presented herein, there are currently 2 pending independent claims and 21 total pending claims in the application. As the original application had 2 independent claims and 30 total claims, Applicant believes no additional fees are due. In the event that any other fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 09-0447 of IBM Corporation.

The present amendment is believed to contain a complete response to the issues raised in the Office Action. Full reconsideration is respectfully requested. If the Examiner should have any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference. In particular, should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is also invited to telephone the undersigned at the number listed below.

Respectfully submitted,

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Dated: April 3, 2007

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